

WHAT IS CLAIMED IS:

1. A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for providing data to an output port, comprising:
- a memory having a plurality of storage elements, each storage element having an input and an output, said input being programmably connectable to either a state machine, microprocessor, or other programmably controllable data source for selection of data for storage therein;
- a first multiplexer having an output, having a plurality of inputs receiving the outputs of said memory, and having a control input for selecting, in response to a control signal, an input for connection to said output;
- a control signal generator for generating a control signal to control said first multiplexer to select said first multiplexer inputs for connection to said first multiplexer output; and
- a clock edge selector circuit for providing, in response to an edge select signal, the output of said first multiplexer to said output port

selectably on either said rising edges or said falling edges of said clock signal.

2.0 The state machine input/output circuit of Claim 1,  
5 wherein said clock edge selector circuit further comprises:

the input of first and second flip-flops coupled to the output of said multiplexer, said first flip-flop changing states on said rising edge of  
10 clock pulse and said second flip-flop changing states on said falling edge of clock pulse;

output of said first and second flip-flops coupled to first and second inputs of a second multiplexer;

15 the control input of said second multiplexer coupled to the output of an edge select register; and

the output of said second multiplexer coupled to said output port.

20 3. The state machine input/output circuit of Claim 1, further comprising a plurality of said input/output circuits, for providing data to a plurality of output ports, wherein said output ports are connected on an  
25 output data bus.

4. The state machine input/output circuit of Claim 1, which is programmable without any prior knowledge of the application device being controlled.

5. A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for passing data from an input port to a sampled output port, comprising:

a clock edge selector circuit having an input coupled to said input port and having an output, for selecting, in response to an edge select signal, data on said input port for provision to said selector circuit output selectably on either said rising edges or said falling edges of said clock signal;

a first multiplexer having an output coupled to a first flip/flop, said multiplexer having two inputs, a first one of said inputs receiving said selector circuit output, and a second one of said inputs coupled to the output of said first flip/flop and to the sampled output port, and having a control input for selecting, in response to a control signal, said first input or said second input for connection to said first multiplexer output;

a control signal generator for generating a control signal to control a second multiplexer to select said second multiplexer inputs for connection to said second multiplexer output;  
5 a memory having a plurality of storage elements, each storage element having an input and an output, said input being programmably connectable to either a state machine, microprocessor, or other programmably  
10 controllable data source for selection of data for storage therein, said memory outputs being connected to the inputs of said second multiplexer, wherein the output of said second multiplexer selects said first input or said  
15 second input of said first multiplexer for connection to said first multiplexer output.

6. The state machine input/output circuit of Claim 5, wherein said clock edge selector circuit further  
20 comprises:

an input to said clock edge selector circuit coupled to the input of a second and a third flip-flop being clocked at said state machine clock rate, said second flip-flop changing  
25 states on said rising edge of clock and said

third flip-flop changing states on said falling edge of clock;

the output of said second and third flip-flops coupled to first and second inputs of a third multiplexer;

the control input of said third multiplexer coupled to the output of a edge select register; and

the output of said third multiplexer coupled to said output of said clock edge selector circuit.

7. The state machine input/output circuit of Claim 5, further comprising a plurality of said input/output circuits, for passing data from an input port to a sampled output port, wherein said inputs are connected on an input data bus and said sampled outputs are connected on an output bus.

8. The state machine input/output circuit of Claim 5, which is programmable without any prior knowledge of the application device being passed to.

9. A state machine input/output circuit responsive to a clock signal having cyclically repeating rising edges and falling edges, for passing output data to an output port, comprising:

a memory having a plurality of storage elements,  
each storage element having an input and an  
output, said input being programmably  
connectable to either a state machine,  
5 microprocessor, or other programmably  
controllable data source for selection of data  
for storage therein;

a first multiplexer having an output, having a  
plurality of inputs receiving the outputs of  
10 said memory, and having a control input for  
selecting, in response to a control signal, an  
input for connection to said output;

a control signal generator for generating a  
control signal to control said first multiplexer  
15 to select cyclically said multiplexer inputs for  
connection to said multiplexer output;

a second multiplexer having a first input and a  
second input, having an output, and having a  
control input for selecting, in response to a  
20 control signal, an input for connection to said  
second multiplexer output, said first input  
being coupled to a predetermined output data  
source, said output being coupled to the control  
input of a first flip-flop being clocked at said  
25 state machine clock rate, said second input

being coupled to the output of said first flip-flop and to the input of a clock edge selector circuit, and said control input being connected to said output of said first multiplexer;  
5 said clock edge selector circuit for providing, in response to an edge select signal, the output of said second multiplexer to said output port selectably on either said rising edges or said falling edges of said clock signal.

10. The state machine input/output circuit of Claim 9, wherein said clock edge selector circuit further comprises:

the input of second and third flip-flops coupled to the output of said second multiplexer, said second flip-flop changing states on said rising edge of clock pulse and said third flip-flop changing states on said falling edge of clock pulse;

output of said second and third flip-flops coupled to first and second inputs of a third multiplexer;

the control input of said third multiplexer coupled to the output of a edge select register;  
25 and

